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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/616,990	07/11/2003	Minoru Kawabata	2003_0956	2773

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EXAMINER	
NATNAEL, PAULOS M	

ART UNIT	PAPER NUMBER
2622	

DATE MAILED: 11/16/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/616,990	KAWABATA ET AL.	
	Examiner	Art Unit	
	Paulos M. Natnael	2622	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 August 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Double Patenting

1. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claims **1-4** rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims **3 and 7** of U.S. Patent No. 6,661,469. Although the conflicting claims are not identical, they are not patentably distinct from each other because allowing the invention defined by claims **1 and 3** of the instant application would result in an unwarranted timewise extension of the monopoly defined by the invention of claim **3,7** of Patent No. 6,661,469, (hereinafter, '469).

Considering claim 1,

a) the claimed double bit change detection circuit for detecting a signal portion in the digital image signal, where a change in graduation between two adjacent pixels is twice a unit of graduation level represented by a digital value, and outputting a signal representing the results of the detection as a double bit change detection signal, is met by a double bit change detection circuit for detecting in the digital image signal, a signal value change which is twice a minimum quantization unit of the digital image signal as a double bit change, and outputting a signal representing results of the detection as a double bit change detection signal; a signal correction circuit for correcting a double bit change portion, which is a portion where the double bit change exists, in the digital image signal to reduce the false contour based on the double bit change detection signal; claim 3 of Patent '469.

b) the claimed signal correction circuit for correcting the signal portion in the digital image signal to reduce the false contour based on the double bit change detection signal, is met by "a signal correction circuit for correcting a double bit change portion, which is a portion where the double bit change exists, in the digital image signal to reduce the false contour based on the double bit change detection signal", claim 3, Patent '469.

Considering claim 2, wherein said signal correction circuit is operable to correct the signal portion in the digital image signal into a portion where there exist two one-bit changes each of which is a signal value change corresponding to the unit of graduation

level based on the double bit change detection signal, is met by the claimed "wherein said signal correction circuit corrects the double bit change portion in the digital image signal into a portion where there exists two one-bit changes each of which is a signal value change corresponding to the minimum quantization unit based on the double bit change detection signal, claim 3, of Patent '469.

Considering claim 3,

a) the claimed double bit change detecting operation of detecting a signal portion in the digital image signal, where a change in graduation between two adjacent pixels is twice a unit of graduation level represented by a digital value, is met by double bit change detecting operation of detecting, as a double bit change portion, a portion where values of adjacent pixels differ by a value which is twice a minimum quantization unit of the digital image signal in an image represented by the digital image signal, of claim 7, Pat. '469.

b) the claimed a correcting operation of correcting the signal portion in the digital image signal to reduce the false contour based on the double bit change detection signal, is met by the claimed "a correcting operation of correcting the values of the pixels in the double bit change portion, to reduce the false contour", of claim 7, pat. '469.

Considering claim 4, wherein said correcting operation comprises correcting the signal portion in the digital image signal into a portion where there exist two one-bit changes each of which is a signal value change corresponding to the unit of graduation level, is

met by, wherein said correcting operation comprises correcting the values of the pixels in the double bit change portion based on results of the detection in said detecting operation such that there exists two one-bit change portions, each of the two one-bit change portions being defined as a portion where a one-bit change exists and the values of the adjacent pixels differ by the minimum quantization unit, claim 8, Pat. '469.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shigeta, U.S. Pat. No. 6,064,456.

Considering claim **1,** Shigeta discloses a "false contour correcting circuit 3 is operated to correct a false contour of the pixel data D and produces a correcting pixel data HD which is applied to the frame memory 4. (col. 4, lines 40-43) "The high-figure bit change detecting circuit 31 is applied with the pixel data D for detecting the change of the high-figure bit of the data at a next field. The pixel data D is a data of 6-bit from the fifth bit of most significant bit (MSB) to the zeroth bit, and the change of the high-figure ***three bits of each pixel data is detected."*** [emphasis added] (col. 5, lines 21-26) The system detects the change of the three bits of each pixel data, not just one bit, and meets the

claimed two bit or double bit change detection. Circuit 3 is illustrated in greater detail in Fig.3. High-figure bit change detecting circuit 31 detects the change of the three bits of each pixel data. The delay circuit, the first, second and third data converting circuits 33,34,35 [which convert the pixel data of 6 bits to a converting pixel data of A, B, and C of 8 bits (see col. 6, lines 31-65)] along with the Selector Control Circuit 36 and Selector 37 constitute the correction circuit.

Shigeta does not specifically disclose that a change in graduation between two adjacent pixels is twice a unit of graduation level represented by a digital value. However, Shigeta

Regarding claim **2**, See rejection of claim 1.

Claims 3 and 4 are method claims of claims 1 and 2, respectively and thus, claims 3 and 4 are rejected for the same reasons as in claims 1 and 2.

Response to Arguments

4. Applicant's arguments filed 8-21-06 have been fully considered but they are not persuasive. Applicant argues against the applied reference Shigeta essentially by repeating the claims. Furthermore, the applicant asserts that it is apparent that the false contour corrected by the change in luminescence in the false contour correcting circuit 3 of Shigeta is not the false control caused by the digital signals processing performed on

a digital image signal [emphasis added] that is corrected by the claimed signal correction circuit. (see Remarks, Page 5) Apparently, the applicant denies here that Shigeta's system operates on the digital signal. However, it is clear from the drawing and detailed explanations the Shigeta's system operates on the digital signal (the input "D").

The applicant also argues the claims do not recite false contour occurring "independent of the type of display device that is used." (see Remarks, page 6) However, again, why or how "false contour" occurs is not recited in the claims. In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., the "false contour" described above with respect to the present invention which may occur independent of the type of display device that is used) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

The applicant appears to argue as well that although the objective of both Shigeta and the invention appear to be similar, the object are "different", contradicting their earlier statement.

The Examiner submits that the process may be different but the objective of Shigeta is clearly to correct "false contour". The term false contour has one and the same meaning as it's well known process in the art. **Shigeta** discloses a false contour correcting circuit 3 (fig.1), which circuit is illustrated in greater detail in Fig.3. Shigeta

discloses a "false contour correcting circuit 3 is operated to correct a false contour of the pixel data D and produces a correcting pixel data HD which is applied to the frame memory 4. (col. 4, lines 40-43) "The high-figure bit change detecting circuit 31 is applied with the pixel data D for detecting the change of the high-figure bit of the data at a next field. The pixel data D is a data of 6-bit from the fifth bit of most significant bit (MSB) to the zeroth bit, and the change of the high-figure ***three bits of each pixel data is detected."*** [emphasis added] (col. 5, lines 21-26) The system detects the change of the three bits of each pixel data, not just one bit, and meets the claimed two bit or double bit change detection. Circuit 3 is illustrated in greater detail in Fig.3. High-figure bit change detecting circuit 31 detects the change of the three bits of each pixel data. The delay circuit, the first, second and third data converting circuits 33,34,35 [which convert the pixel data of 6 bits to a converting pixel data of A, B, and C of 8 bits (see col. 6, lines 31-65)] along with the Selector Control Circuit 36 and Selector 37 constitute the correction circuit. Thus, the correction circuit disclosed in Shigeta performs the claimed double bit change detection circuit for detecting in the digital image signal a signal value change, and the claimed a signal correction circuit for correcting a double bit change portion. The selector 37 then selects the signal using the predetermined method.

Thus, the argument is unpersuasive.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paulos M. Natnael whose telephone number is (571) 272-7354. The examiner can normally be reached on 8AM-4:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Ometz can be reached on (571)272-7593. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

November 12, 2006

PAULOS NATNAEL
PRIMARY PATENT EXAMINER